REMARKS

Claims 1, 3-9, 11 and 12 are pending in the present application, were examined, and stand rejected. In response, Claims 1, 3, 5, 6, 9 10 are amended, no claims are cancelled and no claims are added.. Applicant respectfully requests reconsideration of pending Claims 1, 3-9, 11 and 12 in view of at least the following remarks. Reconsideration and withdrawal of the rejections of record are requested in view of such amendments and the following discussion.

I. Claims Rejected Under 35 U.S.C. §103

The Examiner has rejected Claims 1, 3-9 and 11-12 under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,216,178 issued to Stracovsky et al. ("Stracovsky") in view of U.S. Patent No. 6,128,702 issued to Saulsbury et al. ("Saulsbury"). Applicant respectfully traverses this rejection.

To establish a *prima facie* case of obviousness, the following criteria must be met: (1) there must be some suggestion or motivation to modify the reference or combine the reference teachings, (2) there must be a reasonable expectation of success, and (3) the prior art references must teach or suggest all the claim limitations. (MPEP §2142) For the reasons provided below, the Examiner has failed to establish a *prima facie* case of obviousness in view of the references of record.

Claim 1 is amended to recite the following claim feature, which is neither taught nor suggested by either Stracovsky or Saulsbury, whether reviewed alone or in combination:

> a command sequencer and serializer unit coupled to the array of tag address storage locations, the command sequencer and serializer unit to control a data cache and an eviction buffer located on at least one memory device of an off-chip memory module, the memory controller coupled to the memory module via a memory bus, the command sequencer and serializer unit to cause a current line of data to be written from the command sequencer and serializer unit to the data cache, the command sequencer and serializer unit to cause a previous line of data to be evicted out of the data cache to the eviction buffer located on the memory device.

As correctly pointed-out by the Examiner, Stracovsky differs from the claimed invention and not specifically [sic] teaches a data cache located on the memory module and the command sequencer and serial unit to cause a previous line of data to be evicted out of the data cache to an eviction buffer located on the memory module. (*See*, paper no. 3 of Office Action mailed March 24, 2004.) Accordingly, the Examiner cites Saulsbury, which according to the Examiner, teaches the above-described features of Claim 1 prior to amendment.

Contrary to Applicants invention, as well as Stracovsky, Saulsbury is directed:

> An integrated P/M device 100 in accordance with the present invention to integrate integrated components of the P/M device include a CPU 102, an on-chip memory system 103, a 64-bit data bus 108, a 25-bit data address bus 110, a 32-bit instruction bus 112, a 25-bit instruction address bus 114 and a control bus 116.

> The memory system includes 16 memory blocks 104 and a victim cache 106. (col. 3, lines 46-53.)

Conversely, Claim 1, as amended, recites an off-chip memory module. Furthermore, as indicated by the cited passage of Saulsbury, the memory system includes 16 memory blocks and a victim cache 106. Conversely, Claim 1, as amended, recites a data and eviction buffer per memory device of a memory module. Accordingly, Applicants respectfully submit that the Examiner fails to establish a *prima facie* case of obviousness of Claim 1, as amended, since the combination of Stracovsky in view of Saulsbury fails to teach or suggest each of the features of Claim 1, as amended. Furthermore, Applicants respectfully submit that the Examiner fails to illustrate a suggestion or motivation to modify the teachings of Stracovsky in view the teachings of Saulsbury. Applicants respectfully submit that the lack of such a suggestion or motivation is based on the fact that Stracovsky deals with problems faced by:

> Systems in which many components (processors, hard drive, etc.) must share a common bus in order to access memory presence [sic] there is a high probability of memory access conflicts. (col. 1, lines 37-40.)

Applicants respectfully submit that the teachings of Stracovsky refer to off-chip memory systems, which are generally coupled to a processor and corresponding chipset via a memory bus. Conversely, as indicated above, Saulsbury is directed to an integrated processor/memory device comprising a main memory, a CPU, a victim cache and a primary cache (*See*, Abstract). Accordingly, Applicants respectfully submit that one skilled in the art would not look to a reference such as Saulsbury, which teaches an integrated processor memory device to solve problems associated with off-chip system memory, as described in the Background of Stracovsky. Accordingly, Applicants respectfully submit that the Examiner fails to establish a *prima facie* case of obviousness of Claim 1, as amended, since the Examiner fails to illustrate a teaching or suggestion to modify or combine the reference teachings of Stracovsky in view of Saulsbury and also fails to illustrate a teaching or suggestion of each of the above-recited features of amended Claim 1, based on the combination of Stracovsky in view of Saulsbury. Accordingly, Applicants respectfully submit that Claim 1, as amended, is patentable over Stracovsky, Saulsbury and the references of record, whether viewed alone or in combination. Consequently, Applicants respectfully request that the Examiner reconsider and withdraw the §103(a) rejection of Claim 1.

Regarding Claims 3 and 4, Claims 3 and 4 depend from Claim 1 and therefore include the patentable claim features of Claim 1, as described above. Accordingly, Claims 3 and 4, based on their dependency from Claim 1, are also patentable over the combination of Stracovsky in view of Saulsbury, as well as the references of record. Consequently, Applicants respectfully request that the Examiner reconsider and withdraw the §103(a) rejection of Claims 3 and 4.

Regarding Claim 5, Claim 5 is amended to recite the following claim features, which are neither taught nor suggested by either Stracovsky, Saulsbury or the references of record:

> . . . an eviction buffer coupled to the memory device, the data cache controlled by a plurality of commands delivered by a memory controller over a memory bus, the memory controller including an array of tag address storage locations, the memory controller to write a current line of data to the data cache, the memory controller to cause a previous line of data to be evicted out of the data cache to the eviction buffer located on the memory device.

As indicated above with reference to Claim 1:

> The memory system includes 16 memory blocks 104 and a victim cache. (col. 3, lines 52-53.)

Conversely, Claim 5, as amended, recites a data cache and eviction buffer per memory device of the memory module of Claim 5. Accordingly, Applicants respectfully submit that the Examiner fails to establish a *prima facie* case of obviousness of Claim 5 over Stracovsky in view of Saulsbury, since the combination fails to teach a data cache and victim block from memory device since Saulsbury is limited to a single victim cache that is shared by the memory system. Furthermore, as indicated above, Stracovsky is directed to problems associated with off-chip system memory, whereas Saulsbury teaches an integrated processor and memory device. Accordingly, Applicants respectfully submit that Applicants' amendment to Claim 5 prohibits the Examiner from establishing a *prima facie* case of obviousness of Claim 5, since Claim 5, as amended, recites claim features which are neither taught nor suggested by either Stracovsky or Saulsbury, whether viewed alone or in combination. Consequently, Applicants respectfully request that Claim 5, as amended, is patentable over the combination of Stracovsky in view of Saulsbury, as well as the references of record. Consequently, Applicants respectfully request that the Examiner reconsider and withdraw the §103(a) rejection of Claim 5.

Regarding Claims 6-8, Claims 6-8 depend from Claim 5 and therefore include patentable claim features of Claim 5, as described above. Accordingly, Claims 6-8, based on their dependency from Claim 5, are also patentable over the combination of Stracovsky in view of Saulsbury. Consequently, Applicants respectfully request that the Examiner reconsider and withdraw the §103(a) rejection of Claims 6-8.

Regarding Claim 9, Claim 9 is amended to recite the following claim features, which are neither taught nor suggested by either the combination of Stracovsky, Saulsbury or the references of record:

> an off-chip memory module coupled to the memory controller, the memory module including
> at least one memory device, and
> a data cache including an eviction buffer coupled to the memory device, the data cache controlled by a plurality of commands delivered by the memory

controller, the memory controller writing a current line of data to the data cache, the memory controller to further instruct the data cache to evict a previous line of data from the data cache into the eviction buffer.

As indicated above with reference to Claims 1 and 5, the combination of Stracovsky in view of Saulsbury fails to teach an off-chip memory module that includes at least one memory device having a data cache and eviction buffer located on the memory device. Accordingly, Applicants respectfully that Applicants' amendment to Claim 9 prohibits the Examiner from establishing a *prima facie* case of obviousness of Claim 9 over Stracovsky in view of Saulsbury, since the combination fails to teach or suggest each of the features of Claim 9, as amended. Furthermore, as indicated above, Applicants respectfully submit that the Examiner fails to show a suggestion or motivation to combine the reference teachings since Stracovsky is directed to problems associated with off-chip system memory, whereas Saulsbury teaches an integrated processor and memory device; and hence, is not directed to problems associated with off-chip system memory. Consequently, Applicants respectfully submit that Claim 9, as amended, is patentable over the combination of Stracovsky in view of Saulsbury, as well as the references of record. Consequently, Applicants respectfully request that the Examiner reconsider and withdraw the §103(a) rejection of Claim 9.

Regarding Claims 11 and 12, Claims 11 and 12 depend from Claim 9 and therefore include the patentable claim features of Claim 9, as described above. Accordingly, Claims 11 and 12, based on their dependency from Claim 9, are also patentable over the references of record. Consequently, Applicants respectfully request that the Examiner reconsider and withdraw the §103(a) rejection of Claims 11 and 12.

CONCLUSION

In view of the foregoing, it is submitted that Claims 1, 3-9, 11 and 12, as amended, patentably define the subject invention over the cited references of record, and are in condition for allowance and such action is earnestly solicited at the earliest possible date. If the Examiner believes a telephone conference would be useful in moving the case forward, he is encouraged to contact the undersigned at (310) 207-3800.

If necessary, the Commissioner is hereby authorized in this, concurrent and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2666 for any additional fees required under 37 C.F.R. §§1.16 or 1.17, particularly, extension of time fees.

Respectfully submitted,
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Dated: September 21, 2004

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I hereby certify that this correspondence is being transmitted via facsimile on the date shown below to the United States Patent and Trademark Office.

Nedy Calderon 9/21/04
Nedy Calderon Date